IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

ACQIS LLC, *Plaintiff*,	§	
-v-	§	**1-23-cv-00822-ADA**
SONY GROUP CORPORATION, SONY INTERACTIVE ENTERTAINMENT INC., SONY INTERACTIVE ENTERTAINMENT LLC, *Defendants*.	§	

CLAIM CONSTRUCTION ORDER

The Court held a *Markman* hearing on August 11, 2023. During that hearing, the Court provided its final constructions. The Court now enters those claim constructions.

SIGNED this 6th day of September, 2023.

ALAN D ALBRIGHT
UNITED STATES DISTRICT JUDGE

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Final Construction
#1: "low voltage differential signal (LVDS) [channel]" / "LVDS channel" U.S. Patent No. 8,977,797, Claims 33, 34; U.S. Patent No. 9,529,768, Claims 1, 2, 13, 17; U.S. Patent No. 9,703,750, Claims 1, 2, 5, 7, 10, 12, 21, 24, 31, 34, 35, 44; U.S. Patent No. RE44,654, Claims 20, 21; U.S. Patent No. RE45,140, Claims 14, 15, 17-19, 21, 30, 31, 34-36, 38. Proposed by Defendants	No construction necessary. These terms should be given their plain and ordinary meaning. These terms are not indefinite.	"[a channel for carrying] a signal in accordance with ANSI/TIA/EIA-644 or IEEE 1596.3" or, alternatively, indefinite.	Plain-and-ordinary meaning. Not indefinite.

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Final Construction
#2: "Peripheral Component Interconnect (PCI) bus transaction" / "PCI bus transaction" U.S. Patent No. 9,529,768, Claims 1, 2, 13, 17; U.S. Patent No. 9,703,750, Claims 1, 2, 5, 7, 10, 12, 21, 31, 34, 35, 44; U.S. Patent No. RE44,654, Claim 21; U.S. Patent No. RE45,140, Claims 30, 31, 34. Proposed by Plaintiff and Defendants	"a transaction, in accordance or backwards compatible with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component"	"a transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component"	"a transaction, in accordance or backwards compatible with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component"

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Final Construction
#3: "convey [conveying/conveys/ communicating/communicate/ transmitting] … a Peripheral Component Interconnect (PCI) bus transaction [/of a PCI bus transaction]" U.S. Patent No. 9,529,768, Claims 1, 2, 13, 17; U.S. Patent No. 9,703,750, Claims 1, 2, 5, 7, 10, 12, 21, 31, 34, 35, 44; U.S. Patent No. RE44,654, Claim 21; U.S. Patent No. RE45,140, Claims 30, 31, 34. Proposed by Defendants	Other than "PCI bus transaction," addressed above, these terms do not require construction. Specific recited bits of a PCI bus transaction should be given their plain and ordinary meaning.	"communicating a PCI bus transaction, including all address, data, and control bits"	**"conveying" / "conveys" / "communicating" / "communicate" / "transmitting"**: Plain-and-ordinary meaning • **"[conveying / conveys / communicating / communicate / transmitting] … PCI bus transaction"**: The *EMC* construction for "communicating … PCI bus transaction" applies to these terms. • **"conveying" / "conveys" / "communicating" / "communicate" / "transmitting" specific bits (*e.g.*, address bits, data bits, and/or byte enable information bit) of a "PCI bus transaction"**: The *EMC* construction for "communicating … PCI bus transaction" does not apply to these terms.

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Final Construction
#4: "of a Peripheral Component Interconnect (PCI) bus transaction" / "of a PCI bus transaction" U.S. Patent No. 9,529,768, Claims 1, 2, 13, 17; U.S. Patent No. 9,703,750, Claims 1, 2, 5, 7, 10, 12, 21, 31, 34, 35, 44; U.S. Patent No. RE44,654, Claim 21; U.S. Patent No. RE45,140, Claims 30, 31, 34. Proposed by Defendants	No construction necessary. Putting aside "PCI bus transaction," addressed above, this phrase should be broadened to include its full context—i.e., "address and data [bits] of a Peripheral Component Interconnect (PCI) bus transaction" / "address bits, data bits, and byte enable information bits of a Peripheral Component Interconnect (PCI) bus transaction"—and given its plain and ordinary meaning. "[O]f a" does not require construction.	"from a transaction that is in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component"	Plain-and-ordinary meaning; *see also* the Court's Construction for Term #2 ("Peripheral Component Interconnect (PCI) bus transaction" / "PCI bus transaction")

#5: Claims reciting an "encoded" PCI bus transaction (or, per ACQIS's position, specific bits thereof) in a "serial [bit] stream" or "serial form" or "serially encoded" and Claims reciting a PCI bus transaction (or, per ACQIS's position, specific bits thereof) in a "serial form" or "serial bit stream" U.S. Patent No. 9,529,768, Claims 1, 2, 13, 17; U.S. Patent No. 9,703,750, Claims 1, 2, 5, 7, 10, 12, 21, 31, 34, 35, 44; U.S. Patent No. RE44,654, Claim 21; U.S. Patent No. RE45,140, Claims 30, 31, 34. Proposed by Plaintiff and Defendants	"Encoding" terms, reciting conveying/transmitting *encoded* address and data bits of a PCI bus transaction or *encoded* address bits, data bits, and byte enable information bits, should be given their plain and ordinary meaning, wherein the plain and ordinary meaning of "encoded" is "code representing [the recited bits of] a PCI bus transaction." "Serial" terms, reciting conveying/transmitting (1) address and data bits of a PCI bus transaction, or (2) address bits, data bits, and byte enable information bits, "in [a] serial form," or "serially," or "in a serial bit stream," should be given their plain and ordinary meaning. The *EMC* construction of "[e]ncoded . . . serial bit stream of Peripheral Component Interconnect (PCI) bus transaction" and related terms applies only to certain claims and terms, i.e., "claims reciting an 'encoded' PCI bus transaction" and more specifically, terms that recite	"a PCI bus transaction that has been serialized from a parallel form"	**"encoded"**, **"serial[ly]"**: Plain-and-ordinary meaning *See also* the Court's Construction for Term #2 ("Peripheral Component Interconnect (PCI) bus transaction" / "PCI bus transaction") The *EMC* construction of "[e]ncoded . . . serial bit stream of Peripheral Component Interconnect (PCI) bus transaction" and related terms applies only to certain claims and terms, i.e., "claims reciting an 'encoded' PCI bus transaction" and more specifically, terms that recite (1) "encoded," (2) "serial," and (3) "PCI bus transaction."

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Final Construction
	(1) "encoded," (2) "serial," and (3) "PCI bus transaction."		
#6: "console" U.S. Patent No. 9,703,750, Claims 5, 7, 10, 12, 24, 35, 44; U.S. Patent No. RE44,654, Claims 20, 21; U.S. Patent No. RE45,140, Claims 14, 15, 17, 18, 19, 21, 31, 34. Proposed by Plaintiff and Defendants	"a chassis or enclosure, housing one or more coupling sites, that connects components of a computer system"	"a chassis that connects several components of a computer system"	"a chassis or enclosure, housing one or more coupling sites, that connects components of a computer system"

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Final Construction
#7: "USB" / "Universal Serial Bus (USB) protocol" / "Universal Serial Bus (USB) protocol data" / "Universal Serial Bus (USB) protocol information" U.S. Patent No. 8,977,797, Claims 33, 34; U.S. Patent No. 9,703,750, Claims 7, 24; U.S. Patent No. RE44,654, Claims 20, 21; U.S. Patent No. RE45,140, Claims 15, 18, 19, 21, 34, 36. Proposed by Plaintiff and Defendants	No construction necessary. These terms should be given their plain and ordinary meaning.	"[data/information conveyed according to] the protocols defined in the Universal Serial Bus Specification Revision 2.0 and the prior versions of this standard"	Plain-and-ordinary meaning.
#8: "serial bit channels" / "serial channel" U.S. Patent No. 8,977,797, Claims 33, 34; U.S. Patent No. 9,703,750, Claims 10, 12; U.S. Patent No. RE44,654, Claims 20, 21; U.S. Patent No. RE45,140, Claims 14, 15, 17-19, 21, 30, 31, 34, 35, 36, 38. Proposed by Defendants	No construction necessary. These terms should be given their plain and ordinary meaning.	"a path on which units of information are transferred serially from one component to another"	Plain-and-ordinary meaning.